MEMORY TESTING

Abstract of the Disclosure

A structure comprising a memory chip and a tester for testing the memory chip, and a method for operating the structure. The memory chip comprises a BIST (Built-in Self Test) circuit, a plurality of RAMs (Random Access Memories). A first RAM is selected for testing by scanning in a select value into a RAM select register in the BIST. While the BIST performs a first testing pass for the first RAM, the tester collects cycle numbers of the failing cycles. Then, the BIST performs a second testing pass for the first RAM. At each failing cycle identified during the first testing pass, the BIST pauses so that the content of the location of the first RAM associated with the failing cycle and the state of the BIST can be extracted out of the memory chip. The testing procedures for the other RAMs are similar to that of the first RAM.